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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/800,999	03/16/2004	Nobutaka Kitagawa	250561US2S	1596

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EXAMINER	
KITOV, ZEEV	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/800,999	KITAGAWA, NOBUTAKA	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 2, 4, 6 - 16* is/are rejected.

7)☒ Claim(s) *3 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/16/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 14 and 15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. A reason for that in the following limitation of the claims: "said NPN type bipolar transistor is comprised of a parasitic NPN type bipolar element having a P type region in the first NMOS transistor and N type regions in the source and drain of the second NMOS transistor". The claimed structure is neither illustrated in the Drawings, nor sufficiently explained in the Specification. The Specification provides only description of the Fig. 5 schematic diagram without giving any explanation of the claimed semiconductor structure; it essentially only repeats the claim language (page 19, lines 3 – 14). Since no details are provided the claimed semiconductor structure is totally unclear; it is not clear how the bipolar transistor can function having its base in the P type region of one NMOS transistor and the collector and emitter in the source and drain of the second NMOS transistor. The Claims 14 and 15 have been examined according to the best understanding of the Examiner, i.e. it was assumed that the NPN

type bipolar transistor is comprised of a parasitic NPN type bipolar element having the P type region in the well common to the first NMOS and second NMOS transistors and the N type regions in the source and drain of the second NMOS transistor.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the structure of the NPN type bipolar transistor recited in Claims 14 and 15, which is comprised of a parasitic NPN type bipolar element having a P type region in the first NMOS transistor and N type regions in the source and drain of the second NMOS transistor must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New

Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 6 - 8 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Hulfachor et al. (US 2003/0026054). Regarding Claim 16, Hulfachor et al. disclose all the elements of the Claim including an NPN type bipolar transistor (element 30 in Fig. 1A) having a collector and an emitter connected between a first power supply terminal (Vcc in Fig. 1a) and a reference terminal (GND in Fig. 1A) in the semiconductor device to be protected; a control circuit (elements 220K and C1 in Fig.1A) outputting a control signal in response to a voltage emerging on the first power supply terminal; and a logical circuit having an output terminal (terminal 2 in Fig. 1A) connected to the gate of NESD transistor and to the base of the NPN type bipolar transistor (element 30 in Fig.1a) performing a logical operation based on a voltage on a second power supply terminal in the semiconductor device to be protected and the control signal of the

control circuit (only combination of the voltage on the Vcc power supply line and the output signal of the control circuit on line 2 in Fig. 1A causes activation of the bipolar transistor); the circuit supplies a base current from the output terminal to the base of the NPN type bipolar transistor (through NESD transistor, since the bipolar transistor is the parasitic lateral transistor associated with the NESD transistor) (col. 2, paragraph [0021]).

As per Claim 1, it differs from Claim 16 rejected accordingly by it limitation of a PMOS transistor. Hulfachor et al. disclose the PMOS transistor (element 4 in Fig. 1A) having a drain terminal and a source terminal connected between a base and the collector of the NPN bipolar transistor (through NESD transistor, since the bipolar transistor is the parasitic lateral transistor associated with the NESD transistor, page 2, paragraph [0021]), and supplying a base current to the base of the NPN type bipolar transistor (element 30 in Fig. 1A).

Regarding Claim 2, Hulfachor et al. disclose the resistor (element R1 in Fig. 1A) connected between the base and the emitter of the NPN type bipolar transistor.

Regarding Claim 6, Hulfachor et al. disclose the control circuit (elements 220K and C1 in Fig. 1A) functioning as following: when a voltage higher than a predetermined voltage is applied to said external connection terminal, operating the PMOS transistor upon receipt of that voltage to supply a base current to the NPN type bipolar transistor and, when the voltage on the external connection terminal becomes lower, turning the base current supplied from the PMOS transistor OFF (page 2, paragraphs [0024 – 0025]).

Regarding Claim 7, Hulfachor et al. disclose the control circuit including a resistive element and a capacitor serially connected between the external connection terminal and the reference terminal (elements 220K and C1 in Fig. 1A).

Regarding Claim 8, Hulfachor et al. disclose the resistive element of the control circuit (element 220 k in Fig. 1A) as being connected between the gate of the PMOS transistor (element 4 in Fig. 1A) and the external connection terminal (terminal Vcc in Fig. 1A) and the capacitor (element C1 in Fig. 1A) being connected between the gate of the PMOS transistor and the reference terminal (GND in Fig. 1A).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4, 9, 10, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hulfachor et al. in view of Ker et al. (US 6,465,848), further called Ker 848. Regarding Claim 4, Hulfachor et al. disclose following elements: a control circuit (elements 220K and C1 in Fig.1A) outputting a control signal in response to an over-voltage; a logical circuit (element 4 in Fig. 1A) performing a logic inversion function (the low voltage signal in the input is converted into the high voltage signal in the output) and having an output terminal connected to a base of the NPN type bipolar transistor (element 30 in Fig. 1A) and performing a logical operation based on a voltage on a

power supply terminal of the semiconductor device to be protected and the control signal of the control circuit and to supplying a base current from the output terminal to the base of the NPN type bipolar transistor.

However, its NPN type bipolar transistor is not connected between a data input/output terminal of a semiconductor device to be protected and a reference terminal. Ker et al. disclose the SCR structure (element nSCR in Fig, 5a), which includes an NPN type bipolar transistor (bottom N, P, N layers of the SCR element in Fig. 5a) having a collector and emitter connected between a data input/output terminal of a semiconductor device to be protected (I/) pad in Fig. 5a) and a reference terminal (Vss in Fig. 5a). Both references have the same problem solving area, namely providing the ESD protection for the semiconductor circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Hulfachor et al. solution by connecting its circuit to the I/O pad for ESD protection according to Ker 848, because (I) as Ker 848 states (col. 1, lines 19 – 22), the input-output ports on IC chips are usually designed to include ESAD protect devices or circuits for protecting the devices in IC chips from ESD damage, and (II) such modification will enlarge the business scope of the ESD protection circuits manufacturer.

Regarding Claim 9, Hulfachor et al. disclose the control circuit including a resistive element and a capacitor serially connected between the external connection terminal and the reference terminal (elements 220K and C1 in Fig. 1A).

Regarding Claim 10, Hulfachor et al. disclose the resistive element of the control circuit (element 220 k in Fig. 1A) as being connected between the gate of the PMOS transistor (element 4 in Fig. 1A) and the external connection terminal (terminal Vcc in Fig. 1A) and the capacitor (element C1 in Fig. 1A) being connected between the gate of the PMOS transistor and the reference terminal (GND in Fig. 1A). In the Hulfachor et al. circuit modified according to Kerr et al., the resistive element of the control circuit will be connected between the data input/output terminal and the input of the logical circuit (element 4 in Fig. 1A).

Regarding Claim 13, Hulfachor et al. disclose the logical circuit being configured such, that when a normal operation voltage is supplied to the semiconductor device to be protected, a threshold value is set for retaining the NPN type bipolar transistor in an OFF state (page 2, paragraphs [0024 – 0025]).

Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hulfachor et al. in view of Ker 848 and Ker et al. (US 6,566,715), further called Ker 715. As was stated above, Hulfachor et al. discloses all the elements of Claim 1 and together with Ker 848 all the elements of Claim 4. However, regarding Claims 14 and 15, they do not disclose the parasitic NPN bipolar transistor having its base in the P type region and N type regions in the source and drain of the second NMOS transistor. Ker 715 discloses the NPN type bipolar transistor (shown in Fig. 5B) as a parasitic NPN type bipolar element having a P type region in well (element 32 in Fig. 5B) common to the first NMOS and second transistors and N type regions in the source and drain of the

second NMOS transistor (elements 36 and 38 in Fig. 5B). It further discloses a first NMOS transistor (element Mn3 in Fig. 11) for an input/output buffer connected between the external connection terminal (O/P terminal in Fig. 11) and the reference terminal (VSS in Fig. 11) and a second NMOS transistor (element Mn1 in Fig. 14) connected as the protection circuit for the input/output buffer connected between the external connection terminal and the reference terminal. Both references have the same problem solving area, namely ESD protection for the semiconductor circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Hulfachor et al. solution by modifying the parasitic bipolar transistor structure according to Ker 715, because as Ker 715 states (col. 2, lines 19 – 29), the substrate triggered ESD protection structure has an advantage in performance since it avoids the over-biased gate voltage, which degrades the performance of the ESD protection.

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hulfachor et al. in view of Ker 848 and Co et al. (US 5,173,755). As was stated above, Hulfachor et al. discloses all the elements of Claim 1 and together with Ker 848 all the elements of Claim 4. Regarding Claims 11 and 12, Hulfachor et al. disclose the control circuit including a resistive element. However, they do not disclose a diode serially connected between the external terminal and the reference terminal. Co et al. disclose at least one diode (element 50 in Fig. 2) serially-connected between the external connection terminal (terminal PAD in Fig. 2) and the reference terminal (GND

in Fig. 2). Both references have the same problem solving area, namely providing the ESD protection for the semiconductor circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Hulfachor et al. solution by adding the diode according to Co et al., because as Co et al. state (see Abstract), presence of the diode allows to determine the turn-on voltage of the circuit.

Allowable Subject Matter

1. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. A reason for that is in the claim limitation of presence of NMOS transistor connected between the base and emitter of the NPN bipolar transistor. Such limitation was not found in the collected prior art of the record.

2. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. A reason for that is in the claim limitation of the NOR circuit performing logic operation based on the power supply voltage and the control signal. Such limitation was not found in the collected prior art of the record.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571)

272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (703) 872-9306 for all communications.

Z.K.
05/06/2005

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